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TsEM DIGITAL ELECTRONIC COMPUTER

- USSR -

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TsEM Digital Electronic Computer

[Following is a translation of an article by G.A.Mikhaylov, B.N.Shitikov, N.A.Yavlinskiy in Problemy kibernetiki (Problems of Cybernetics), No. 1, Moscow, 1958, pages 190-202.]

Introduction

There is an acute need for medium class electronic computers together with the large computers designed for equipping calculating centers. The cost and expenses in operating such computers is eight to ten times less than the cost of the large computers, and their technical characteristics fully meet the requirements of scientific research institutes and planning design organizations. The M-2 computer of such type of the Academy of Science's Laboratory of Control Mechanisms is designed on the parallel principle (L1) while the "Ural" serial computer uses a magnetic drum in the capacity of memory device (L2). The serial type computer described in this article has operative storage in ultrasonic lines of delay.

The TsEM-1 digital electronic computer belongs to

medium class computers. It was designed in 1953 to solve the mathematical problems of current institute research topics. The operating experience of this machine confirms that inexpensive, reliable computers, having less productive capacity than large computers, serviced in 'round-the-clock operation by three to four technicians and one engineer, are fully justified. Many institutes and design offices are quite competent to develop and create computers of this type. But if our industry organizes the production of separate computer parts, then the assembly and adjustment of computers by operating personnel is greatly simplified and the application of computer technique will advance more rapidly and yield a greater economic effect.

In working principle digital computers are divided into two classes: computers of parallel action and computers of serial action. In parallel action type computers the positional principle of number representation is applied while the operations with numbers are performed simultaneously in all digits. In the serial action computers, the numbers are represented by a transient sequence of pulses and the arithmetic operations are performed in series digit after digit.

In practise this means that in the parallel action machines per unit of time a larger number of operations

is performed than in the serial computers. This comparison has sense, of course, if the structural electronic parts are identical in action speed. On the other hand, the serial action machines require less equipment. The cost of the serial action computers is thus less than that of the parallel machine.

1. General Data on the Computer

The TsEM-1 digital electronic computer is characterized by the following specifications:

(1) the machine is serial action;

(2) the order coding system is the two-address type with reference of the result to the place of the second number;

(3) the computer operates with 30-digit binary numbers, the 31st digit being used for recording the number binit;

(4) all the numbers introduced in the computer must satisfy the condition $0 \leqslant |x| \leqslant 1 - 2^{-30}$ and are represented in the machine in the form of a fraction with a fixed point; negative numbers are represented by a complementary code;

(5) the storage devices are: operative memory in ultrasonic delay lines (mercury tubes), external memory in a magnetic drum; operative memory capacity is 496

numbers or orders (31 tubes each with 16 codes); the external memory capacity is 4096 numbers or orders;

(6) the computer operates at an internal cycle rate of 512 kc, the average speed in performing operations being:

addition or subtraction . . . . 495 orders/sec,

multiplication or division . . . 232 orders/sec;

(7) used in the computer are about 1900 tubes (crystallic devices are not employed), and power consumption is about 14 kwt,

In the TsEM-1 computer the following language of orders is used: addition (S), subtraction (V), multiplication (U), division (D), multiplication and division by whole powers 2 (shifting to the right and to the left by K digits, P and L), logical digital multiplication (A), carry-over of numbers (N), conditional switching to plus sign (B) to minus (M), tape reading input (Ch), tape recording output (Z).

The TsEM-1 machine was originally designed as a single address type. In the course of designing, on the suggestion of Academician S.A.Sobolev, a two-address system of order coding was applied. In the two-address order, the operation name and address of two numbers are recorded, and the place of the second number is referred to in the

result. In practice the same number of actions are coded in it as in the three-address order, but the number of digits in the code of such an order is 1.35 to 1.4 times less than in the three-address type. Such a method of coding makes it possible to raise the computing rate in comparison with the single-address variant and affords substantial advantages in the use of the storage device.

For convenience of programming, so-called attributes have been introduced in the TsEM-1 computer. By means of the attributes designated by the letters $\alpha, \beta, \gamma, \delta, \varepsilon$ and ξ, a number of extremely valuable order modifications is realized (see appendix 1, p. 3, table 2).

For the realization of such order modifications, a small number of additional elements was required in the computer circuit, but at the same time its logical possibilities are expanded, the volume of programs is reduced, i.e. the operative memory is more effectively used. The TsEM-1 structure of orders has the form shown in Fig. 1.

2. Principal Computer Devices

The functional block diagram of TsEM-1 (Fig.2) gives an idea about the machine's structure. An automated telegraph set of the STA-35 type, operating in an input-output sender, is used as the computer's input-output

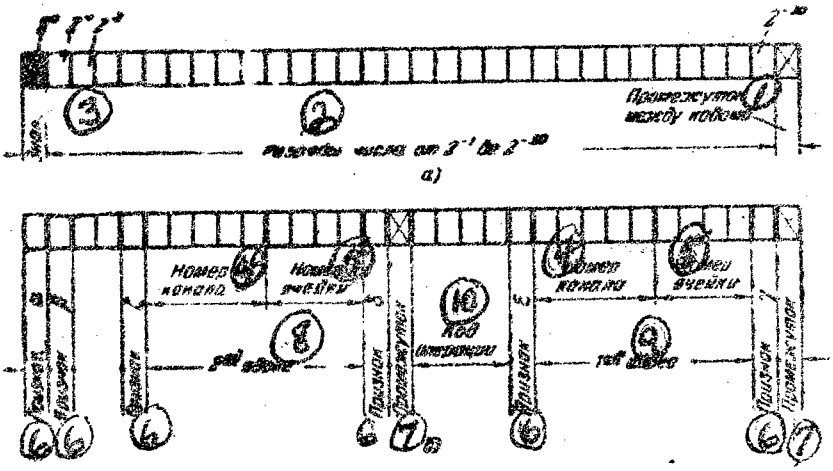


Fig.1 Structure of numbers and orders in TsEM-1:

a) number code; b) order code.

1. space between codes
2. digits of numbers from 2^{-1} to 2^{-30}
3. sign
4. number channel
5. number cell
6. attribute
7. space
8. 2nd address
9. 1st address
10. code of operations

device. The input of a program to the computer is accomplished by means of a paper tape with five tracks. Every decimal digit is represented by holes coded in the decimal binary system. The problem solution result is printed by

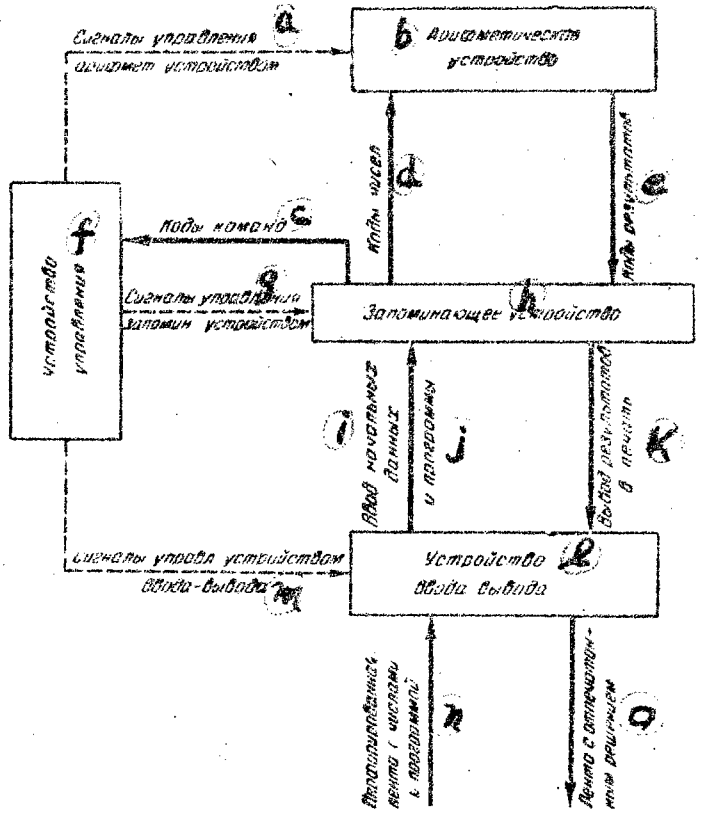


Fig 2. TsEM-1 Block Diagram

KEY:

a -control signals to arithmetic circuit
b - arithmetic circuit
c- order codes
d - number codes
e -result codes
f - control unit
g - control signals to memory

Fig. 2. (KEY continued)

h - storage device
i - input of initial data
j - and programs
k - output of results to print
l - input-output device
m - control signals to input-output device
n - perforated tape with numbers and programs
o - tape with printed results

the telegraph set in the decimal system of numeration and can be simultaneously put out in perforated tape in the decimal binary system. Such an output device makes it possible in a number of cases to use the perforated tape as an external storage device. The results of intermediate calculations in solving problems requiring the recall of data in large volume can be put out on perforated tape and

after that again put into the machine for use. Such a method was in its time used in conversion of a matrix of 100 order since the operative memory capacity was insufficient for storage of the program of conversion and numbers of the matrix.

The storage device (SD) consists of 31 channels. In each channel is an electroacoustical line of delay--a mercury tube (Fig.3). The head of the mercury tube is shown in Fig.4. In one channel are placed 512 pulses, which correspond to 16 numbers or orders of 32 digits each. The pulse conversion time in the channel, the large cycle, amounts to 1000 microseconds. The operation of SD and all the remaining computer units is constructed on the basis of pulses of negative polarity, having an amplitude of 20 to 40 v and width of about 1 microsecond. The generator of high frequency oscillations, which converts pulses into packages of high frequency oscillations with a carrier frequency of 12 Mc, is fixed directly to the transmitting end of the mercury tube. Arranged at the receiving end is the first cascade of amplification of high frequency oscillations. The remaining elements: two high frequency amplification cascades, a detector, videoamplifier, a circuit maintaining the circulation of pulses, out and in pulse gates — are assembled in the

form of a separate unit shown in Fig.5. Separately shown in Fig.6 is one of this unit's assemblies, the synchronization assembly. In this assembly is carried out the strobing of pulses that circulate in the channel, with synchronization pulses which set the operating rhythm of all machine units. The synchronization assembly provides for operation even in case when the pulse being subject to strobing is narrow and does not encompass in width the synchronization pulse corresponding to it.

The arithmetic circuit (AC) performs arithmetic and logical operations. The basis of the TsEM-1 arithmetic circuit consists of:(1) an adder accumulator (an adding element, accumulator (A) and shift circuit);(2) multiplicand accumulator (M); (3) multiplier and divisor accumulator (K); (4) quotient accumulator (Q). Short mercury lines of delay are used in the capacity of accumulators. The tube heads are made the same as are those in the storage device. The basic characteristics of these tubes are given in Table 1.

The arithmetic circuit performs all arithmetic and logical operations. The functional circuit of the arithmetic unit is given in Fig.7.

When operations are performed that fit in a single cycle (S,V,N,B,M), the adder accumulator operates, in

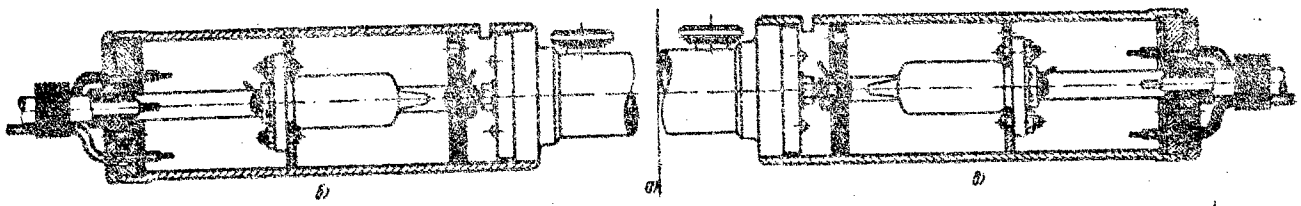
Table 1

Basic Characteristics of Short Mercury Tubes

Characteristics of accumulators	A adder	M multiplicand	K multiplier	Q quotient	P order
number of delayed pulses	30	30	31	32	31
mercury column length in mm	84	84	86.8	89.6	86.8
mercury column diameter in mm	19	19	19	19	19
Time of delay in microseconds	58.6	58.6	60.55	62.5	60.55

which the results of the operation are formulated. To perform multiplication, the multiplier is placed in the multiplier accumulator and the multiplicand in accumulator M. A shift is made at the same time, of the multiplier to the left and the multiplicand to the right. Partial products are formulated in accumulator M, while checking of multiplier digits, beginning from the senior after the point, is performed in accumulator K. Partial products accumulate in adder A.

Performance of the division operation takes place as follows: the dividend and divisor are sent respectively to accumulators A and K, after which the subtration or



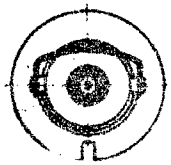


Fig.3. Electroacoustic delay line:
a - mercury tube
b - generator unit
v - amplifier unit

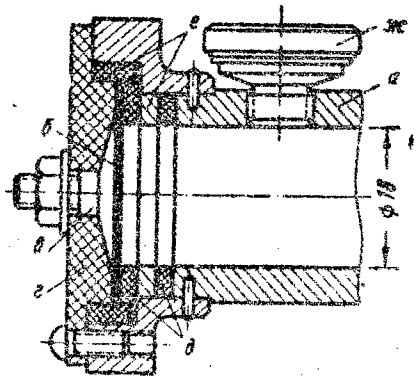


Fig.4. Mercury tube head design:
а- steel tube
b- quartz plate
в- contact screw
г- flange
д- rubber sealing rings
е- space rings
ж- funnel-expander

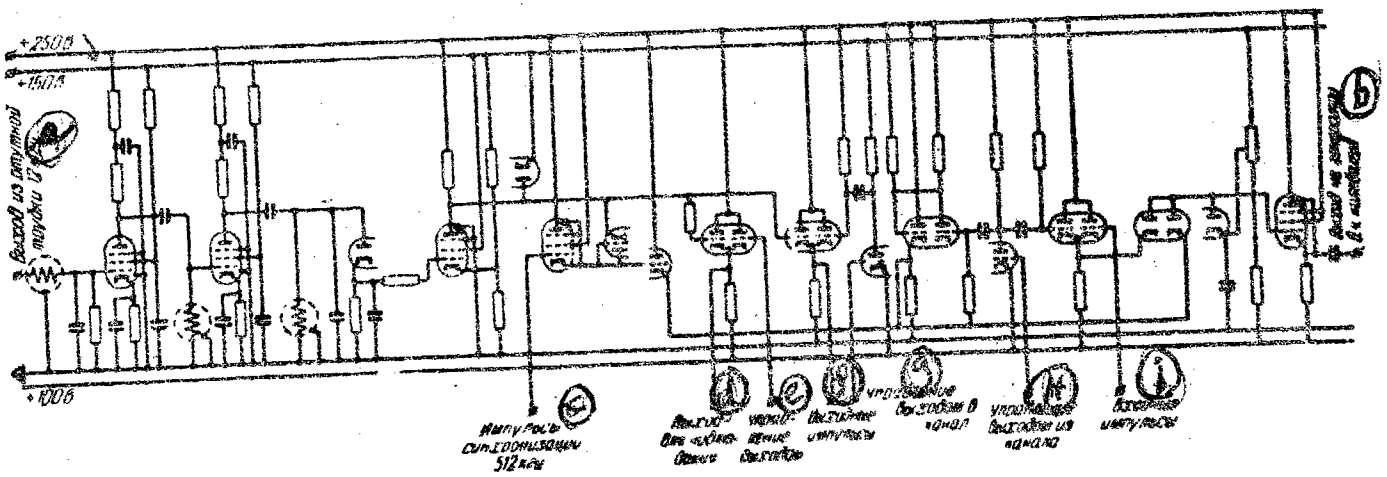


Fig.5. Electronic circuit of storage unit channel

KEY:

a - output from mercury tube 12 Mc
b - output from generator of high frequency oscillations
c - pulses of synchronization 512 kc
d - output for observation
e - output control
f - output pulses
g - control of output in channel
h - control of output from channel
i - input pulses

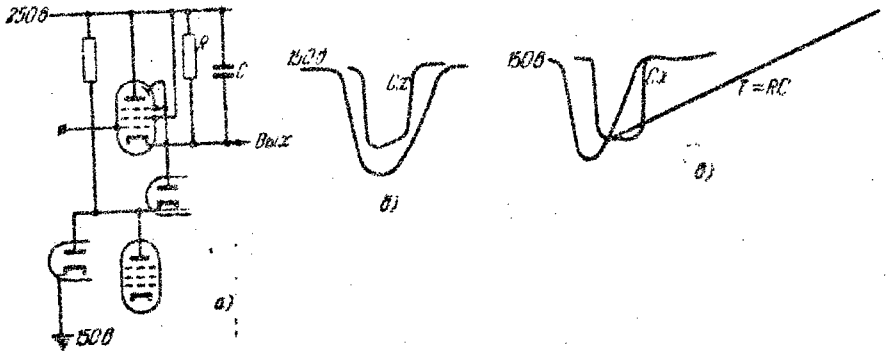


Fig 6. Electronic circuit of storage unit's synchronization assembly
a - assembly circuit
b - operation with wide signal
в - operation with narrow signal

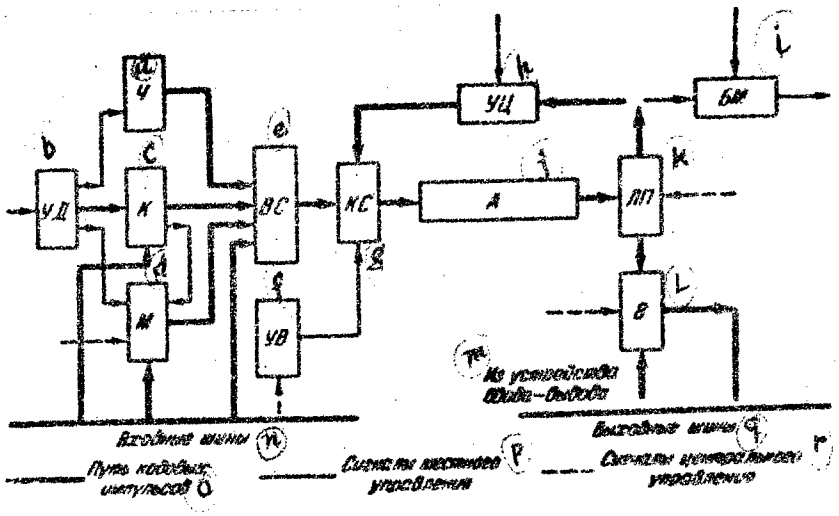


Fig 7. Functional circuit of arithmetic element in TsEM-1:

A - result accumulator; CA - combination adder; S - left and right shift unit; CC - circulation control unit of codes in accumulator adder; AI - adder input unit; B - output unit of adder; K - multiplier and divisor accumulator; M - multiplicand accumulator; Q - quotient accumulator; DU - division and multiplication local control unit; SC - sign-checking unit;SL - local control of subtraction.

English equivalents:

a - Q ; b - DU ; c - K; d -M ; e - AI ; f - SL ; g - CA; h - CC ; i - SC ; j - A ; k - S ; l - B ; m - from input-output device; n - input buses ; o - route of code pulses; p - local control signals ; q - output buses ; r - central control signals.

addition of the divisor depending on the sign of the remainder. The quotient is formed in the special Q accumulator with subsequent dispatch of it to accumulator A.

In the TsEM-1 computer multiplication is performed with round-off of the product, i.e. the product has the

same number of digits as the multiplicand or multiplier. The circuit adopted secures a 10 to 15 % increase of speed in performance of arithmetic operations.

The control unit (CU) performs two basic functions: (1) sets the operating rhythm of all elements and (2) secures the performance of those actions from which is formed performance of each order and transition from one program order to another.

The operating rhythm is set by synchronization pulses having a repitition frequency of 512 kc. The master generator is the source of synchronization pulses. By timing synchronization pulses in a binary scaler, segments of time are separated corresponding to 32 pulses of the number or order code, the small cycles, and further, time segments corresponding to 16 consecutive codes (512) pulses, the large cycles. In each small cycle, the pulses are especially distinguished that correspond to the junior (2^{-31}) and senior (20) digits which are used for commutation and formation of control signals. All switchings accomplished by the control unit are performed in digit 2^{-31} at the junction of adjoining cycles. The presence of a special digit for switchings, not occupied by number pulses, makes it possible to employ in the CU elements not distinguished by high speed action.

The two-address order is performed by the computer in four times: (0) transfer of order from SD to the CU, (1) transfer of first number from SD to AC; (2) transfer and performance of operation required of second number from SD to AC; (3) transfer of result from AC to SD. In the first three times the principal action, selection of the number or order from SD, is preceded by two others: determination of the address of the number or order itself in the SD control unit and awaiting the moment the wanted code appears at the SD output. In the last time, the second address determined in the preceding time, is used once again. One small cycle each is expended in the selection (or dispatch) of the number and in determination of its address; from 0 to 15 cycles in the first three times and 15 cycles in the last time are spent in waiting. In arithmetic actions performed in the second time, the expenditure is from one small cycle when performing orders S,V,N,A coinciding with the selection cycle, to two large cycles in multiplication and division (see Table 1). The address indicating the SD position of the order being filled, is obtained by rating in a special counter the number of performed orders. To the reading of this counter a unit is added after performance of each order and the number of the next order is thus received. By means of conditional orders the readings

rof counters can be replaced by a new order address and be transferred by a leap from one unit of the program to another.

Controlling the rotation of times and separate actions forming each time, the control unit performs the commutation in the computer, securing the performance of operatinns indicated in the order. For this purpose the part of the order in which the operation name has been coded, is sent to the CU functional circuit. Decoding the order, this circuit develops the signals that accomplish the necessary switchings. A series of switchings is performed by signals general for several orders. For example, the entry of the first number in the adder controls the signal general for the operations S,V,N,U,P,B,M, while the entry of the result in the SU controls a signal referring to operations S,V,N,L,D,A. But each order in the second time has at least one signal that distinguishes it from all the others.

3. Characteristics of the Solution of Circuit and Technical Problems in TsEM-1

All the devices in the TsEM-1 are formed of elements widely applied in electronics and communications engineering: in the arithmetic and control circuits radio tubes and radio parts of normal series are employed, in

the SU are mercury delay lines, in the input-output unit an automated STA telegraph set. In all only a few tube models are used: 6H8,6X6 and 6P9 in the AC and CU and in addition to them a negligible number of 6H1P and 6Zh4 in the SD. Semiconductor devices were not employed at all in view of their absence at the time the computer was designed and constructed. The simple substitution of 6X6 diodes by semiconductor diodes of the DGTs model would reduce the number of the computer's tubes by 30 to 35 % without any other reconnection.

The principle of grouping circuits of one and two-tube plug-in units has been widely applied in the TsEM-1. Direct not capacitance connection between circuit elements was employed everywhere it proved possible, which permitted excluding from the circuit transitional circuits and elements of level fixing (constant component preservation). Such a solution was facilitated also by the circumstance that cathode repeaters insensitive to the spread of static tube characteristics, were widely applied as circuit elements. In particular, the circuit's most widespread element, the gate is executed in the form of a doubled cathode repeater. This became possible because of the selection of negative polarity for pulses and the majority of control signals. At the same time the

negative polarity was favorable for obtaining signals with a steep forward front, in the amplifying and forming circuits. All this permitted reducing the number of tubes in the machine. Comparing the TsEM-1 with the English computer EDSAC of the same class, one is readily convinced that the number of tubes in the latter is 1.75 times greater than in the computer described. In the TSEM-1 there are in all only four levels of anode voltage: 100, 150, 200 and 250 v.

A number of other characteristics in the structure of the AC circuit were noted above.

4. Performance Times of Basic Operations by STA

The machine time spent in solution of a problem consists of the following components: (1) the program and number input time and results output time; (2) the time spent directly in computations.

The input of the program and numbers is done through a telegraph set or photoelectric input. The program input speed is 65 orders per minute, the speed of input of decimal numbers with translation to the binary system is 40 numbers per minute. To fill all 496 cells of the operative SU with orders by means of STA requires less than eight min., and with numbers about 12 min. The photoelectric input applied in the TsEM-1 reduces the

loading time ten to twelve-fold. The output of problem solution results is accomplished by means of the same STA and with the same speed as the input of numbers.

The time necessary for the performance of calculations can be estimated as follows. The order filling consists of four times: (in small cycles or s.c.)

zero time -	substitution of order number awaiting order entry from SD and its transfer to accumulator P	- 1 s.c. from 1 to 16
first time -	transfer of order's first part to CU sender	1
second time -	waiting on the first number from SD	from 1 to 16
	transfer of order's second part to CU sender	1
	the duration of the second time is determined by the order's content	
third time -	awaiting and transmission of results to SD	16 s.c.

On the basis of this estimate the minimal time corresponding to a favorable arrangement of addresses in the orders and the maximal time corresponding to unfavorable arrangement, required to fulfill the order can be determined. After completing simple calculations, we derive the data of Table 2.

The time required for the performance of calculations in a given program, depend on the program structure,

i.e on the correlation in it of the number of orders of 1,2,3 and 4th group. As working practice shows, the orders of the 1 to 3 group amount to 80 per cent of all orders, which the 4 group accounts for only 20 per cent. At the same time the average speed of the TsEM-1 can be defined as 400 operations per second.

Table 2

Time Required to Perform Orders and the Order Performance Speed

Order group	Order name	favorable arrangement		unfavorable arrangement	
		order performance time, micro-seconds	number of orders filled in 1 sec.	order performance time micro-seconds	number of orders filled in 1 sec.
1	B,M	1.375	727	3.25	308
2	S,V,N,A	1.375	727	4.184	239
3	L,P	1.375	727	4.125	242
4	U,D	3.312	302	6.125	163

Conclusion

The TsEM-1 computer has been in operation since November 1953. During this period many problems related to varies fields of institute research have been solved. Diversified problems were solved: ordinary differential equations and systems of such equations, matrix conversion,

computation of definite integrals and varied kind of functions.

In the computer investigations have been conducted in the composition of programs from standard subprograms with automatic trimming of addresses in them, and also in the automatic selection of scales in solution of problems that require calculations with a large number of digits.

The three-year experience of computer operation give grounds for drawing the following conclusions:

(1) A serial action computer can be constructed with a minimum of equipment, having adequate calculating speed. Such machines which meet the needs of scientific research institutes and planning design offices can be built with the resources of a small group of engineers and assemblers (seven to eight persons).

(2) Computers with minimal set of orders afford the possibility of simplifying the programming and applying the simplest computer structural circuit.

(3) The two-address system of coding makes programming convenient and is most economical from the viewpoint of utilizing the machine elements.

(4) The use of attributes, while not increasing the machine's cost practically, expands the computer's logical possibilities.

(5) The application of conductive connection between elements made it possible to construct the machine's circuit most economically without using excess elements.

APPENDIXES

1. The Structure of Orders

The code of orders as well as the code of numbers consists of 32 binary digits which are subdivided into the following groups:

The digits 2^{-16} — 2^{-19} , so-called "functions", contain the designation (code) of the operation (addition, subtraction and so forth).

The digits 2^{-5} — 2^{-13}, the so-called "second address", serves for representation of the memory cell number of SD from which proceeds the second number (except L and P) and in which is placed the result (except L,P, B,M).

The digits 2^{-15} and 2^{-30}, the so-called "switching digits", are free digits, at the moment of whose passage switchings are performed in the CU.

The digits 2^{0} — 2^{-2}, — 2^{-4} and 2^{-20}, 2^{-14} and 2^{-30} , the so-called "code letters", serve for representation of attributes on the basis of which order content is changed.

The digits 2^{-21} — 2^{-29}, the so-called "first address", serves for representation of the memory cell

number of SD from which the first number proceeds.

2. Table of Orders

Serial number	Order	Operation code	Operation result	Name of order and content of operation performed by it	Remarks
1	2	3	4	5	6
1	Sab	1111	(a)+(b)	Addition:add number of cell "a" to number of cell "b"	Operation results enter cell "b" replacing former code in it. In cell "a" code is retained.After operation adder is cleared.
2	Vab	0111	(a)-(b)	Subtraction: subtract from number of cell "a" the number of cell "b"	
3	Uab	1110	(a)·(b)	Multiplication:multiply the number of cells"a" and "b"	
4	Dab	0110	(a):(b)	Division:divide the number of cell "a" by the number of cell "b"	
5	Nab	1011 0011	(a)→(b)	Forwarding: place number of cell "a" in cell "b"	
6	Aab	1010	(a)∧(b)	Digital logical multiplication: the result contains units only in those digits, in which both numbers have units, in all the remaining digits -zeros.	
7	Lab	1101	$(a)\cdot 2^{-(b+1)}$	Shift to left: the number taken from cell "a" is shifted	

				leftward by (b+1) digits (without blocking overflow)	Results remain in the adder; "b" is not the address; $0 \leq b \leq 15$
8	Pab	0101	$(a) \cdot 2^{(b+1)}$	Shift to right: the number taken from cell "a" is shifted rightward by (b+1) digits	
9	Bab	1001	$(a) \geqslant 0$	Conditional switching to the "+" sign: if the number $(a) \geqslant 0$, then a transition is made to the order from cell "b"; if $(a) < 0$, then the order next in sequence is performed	codes in cells "a" and "b" are retained. The adder is cleared after the operation
10	Mab	0001	$(a) < 0$	Conditional switching to the "—" sign: if the number $(a) < 0$, then a transition is made to the order from cell "b"; if $(a) \geqslant 0$, then the order next in sequence is performed	
11	Chab	0100		Input of codes in mercury storage device (reading) from input tape or magnetic drum	is examined more in detail in appendix 4
12	Zab	1100		Output of codes from mercury storage device (writing) on tape, perforated tape or magnetic drum	

3. Attributes

The following modifications of orders by means of attributes are provided for:

Serial number	Attribute	Number equivalent	Modification content	Orders with which used	Orders with which not used
1	2	3	4	5	6
1	α	2^{0}	Prohibit clearing of adder at end of the operation	S,V,N,B, U,D,A,M	L,P
2	β	2^{-1}	Prohibit dispatch of results from AC to SD and erasure of code in cell with second address	S,V,N,U, D,A	L,P, B,M
3	γ	2^{-30}	Dispatch of first number to adder with opposite sign	S,V,N,L P,B,M	U,D, A
4	δ	2^{-14}	Receipt of result with opposite sign	U,D,A	S,V, N,L, P,B,M
5	ϵ	2^{-20}	Dispatch of zero to AC instead of the first number and release of first address	S,V,N,L, P,B,M,A	U,D
6	ζ	2^{-14}	Dispatch of zero to AC instead of the second number and release of the second address	S,V,B,M, D	N,L, U,P, A

Footnote. Only α is used with order Z. Attributes are not used with order Ch.

The attributes can be used separately as well as

in the form of combinations of two, three and more letters. Consequently, the combination

$$\sum_{m=2}^{m=6} C_n^m = C_6^2 + C_6^3 + C_6^4 + C_6^5 + C_6^6 = 57$$

is possible. A series of combinations is, however, excluded from this number because, firstly, the attributes δ and γ, ε and ξ, γ and ε, δ and ξ are incompatible and secondly, a prohibition is imposed on combinations with β not having α. For practical applications, therefore, only the combinations $\alpha\beta$, $\alpha\gamma$, $\alpha\delta$, $\alpha\beta\gamma$, $\alpha\beta\delta$, $\alpha\varepsilon$, $\alpha\xi$, $\gamma\xi$, $\delta\varepsilon$, $\alpha\beta\varepsilon$, $\alpha\gamma\xi$ and, it stands to reason, α, γ, δ, ε and ξ remain. The combinations $\alpha\beta$, $\alpha\gamma$, $\alpha\delta$, $\alpha\beta\gamma$, $\alpha\beta\delta$ are most useable. Paragraphs 5 and 6 of Table 2 additionally limit the application of all these combinations with these or those orders. The advantages derived on account of the attributes are nevertheless very substantial.

4. Input and Output Orders

Code input to the operative SD is possible from two sources: from the perforated tape and the magnetic drum. Code output from the SD is possible also in two directions: on the magnetic drum and on perforated tape or teletype tape (or perforated tape and printed tape together).

The input of codes, order Ch, takes place with participation of the adder switched in for digital logical

addition (0 ∨ 0 = 0; 0 ∨ 1 = 1; 1 ∨ 0 = 1; 1 ∨ 1 = 1) and therefore cleared after each order. In performance of order 3, the adder does not participate.

The orders for operation with perforated tape, represented in the form $Cha_1b_1a_2b_2$, $Za_1b_1a_2b_2$, designate:

$Cha_1b_1a_2b_2$ - to read through in perforated tape a line of five binary digits and place it in the a_2b_2 cell, in digits 2^0 to 2^{-4};

$Za_1b_1a_2b_2$ - to represent in perforated tape a group of five binary digits or print the symbol (digit, letter, sign) corresponding to it on telegraph tape, prepared by the preceding order 3, and prepare for printing digits 2^0 to 2^{-4} of cell number "a_2b_2". The first address in these cells is not used. By switching from the panel, the orders can be shifted to operation with six groups of digits and not with one as described above.

The orders for exchange of codes by the basic SD and drum written in the form $Ch^{\gamma\xi} a_1b_1a_2b_2$ and $Z^{\gamma\xi} a_1b_1a_2b_2$ designate:

$Ch^{\gamma\xi} a_1b_1a_2b_2$ - to carry over from drum section ξ with (b_1+1) groups each group of 16 codes; selection from the drum to begin with group a_1, placement of codes in the SD to begin from a_2b_2 cell;

$Z^{\gamma\xi} a_1b_1a_2b_2$ - to represent in drum section ξ

$(b_1 + 1)$ groups each group of 16 codes; selection of codes from SD to begin from a_2b_2 cell; recording of the groups on the drum to begin from group a_1.

In these orders the attribute γ indicates the mode of operation with the drum. The address a_1, b_1 and ξ can assume the value $0 \leqslant a_1 \leqslant 31$; $0 \leqslant \xi \leqslant 7$; $0 \leqslant b_1 \leqslant 15$. In this way, by means of the orders Ch and Z alone from 16 to 256 codes can be removed from or recorded on the drum. The full capacity of all eight sections of the drum amounts to 4096 codes.

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END

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